COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims.

1. (Canceled)

2. (Currently Amended) ~~The~~ A semiconductor device ~~of claim 1~~ comprising:

a substrate of a first conductivity type, the substrate including a plurality of trenches;

a first region of a second conductivity type adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including a channel region adjacent to the trenches;

a second region of the second conductivity type, wherein the second region is in electrical contact with the first region, and the second region extends to a second depth that is deeper than the first depth and shallower than the trenches;

a gate structure in the plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material that has a first thickness at a sidewall of the trench and a second thickness at a bottom of the trench, the second thickness being greater than the first thickness, and wherein the conductive gate extends to a depth that is deeper than the first depth and shallower than the second depth; and

a third region of the first conductivity type atop the first region, wherein a voltage on the conductive gate controls a current flow from the third region through the first region to an underlying portion of the substrate.

3. (Currently Amended) The semiconductor device of claim [[1]] 2, wherein the substrate comprises a first semiconductor layer atop a semiconductor substrate that is more heavily doped than the first semiconductor layer, wherein the trenches extend into the first semiconductor layer.

4. (Original) The semiconductor device of claim 3, wherein the substrate further comprises a second semiconductor layer atop the first semiconductor layer, wherein the

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second semiconductor layer is more lightly doped than the first semiconductor layer.

5. (Currently Amended) ~~The~~ A semiconductor device ~~of claim 4~~ comprising:

a substrate of a first conductivity type, wherein the substrate comprises a first semiconductor layer atop a semiconductor substrate and a second semiconductor layer atop the first semiconductor layer, wherein the semiconductor substrate is more heavily doped than the first semiconductor layer, the second semiconductor layer is more lightly doped than the first semiconductor layer substrate, and a plurality of trenches in the substrate extend into the first semiconductor layer;

a gate structure in the plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material that has a first thickness at a sidewall of the trench and a second thickness at a bottom of the trench, the second thickness being greater than the first thickness;

a first region of a second conductivity type adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including a channel region adjacent to the trenches, wherein [[:]] the first region forms a first junction with the second semiconductor layer;

a second region of the second conductivity type, wherein the second region is in electrical contact with the first region, the second region extends to a second depth that is deeper than the first depth and shallower than the trenches, and the second region forms a second junction with the first semiconductor layer; and

a third region of the first conductivity type atop the first region, wherein a voltage on the conductive gate controls a current flow from the third region through the first region to an underlying portion of the substrate.

6. (Currently Amended) The semiconductor device of claim 3, wherein the voltage on the conductive gate controls a current flow from the third region through the first region and through the first semiconductor layer to the semiconductor substrate.

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7. (Currently Amended) ~~The~~ A semiconductor device ~~of claim 1~~ comprising:

a substrate of a first conductivity type;

a gate structure in a plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material

that has a first thickness at a sidewall of the trench and a second thickness at a bottom of the trench, the second thickness being greater than the first thickness;

a first region of a second conductivity type adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including a channel region adjacent to the trenches;

a second region of the second conductivity type, wherein the second region is in electrical contact with the first region, and the second region extends to a second depth that is deeper than the first depth and shallower than the trenches; and

a third region of the first conductivity type atop the first region, wherein a voltage on the conductive gate controls a current flow from the third region through the first region to an underlying portion of the substrate, wherein

the substrate comprises a layer in which the trenches reside, the layer having a graded dopant profile such that a concentration of dopants of the first conductivity increases with depth in the layer.

8. (Currently Amended) The semiconductor device of claim [[1]] 7, wherein the substrate comprises a series of implantations having varying depths and dopant concentrations such that ~~dopant~~ the concentrations of the dopants of the first conductivity increase with depth in the substrate.

9. (Currently Amended) ~~The~~ A semiconductor device ~~of claim 1~~ comprising:

a substrate of a first conductivity type;

a gate structure in a plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material that has a first thickness at a sidewall of the trench and a second thickness at a bottom of the trench, the second thickness being greater than the first thickness;

a first region of a second conductivity type adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including a channel region adjacent to the trenches;

a second region of the second conductivity type, wherein the second region comprises a series of implantations at varying depths, is in electrical contact with the first region, and extends to a second depth that is deeper than the first depth and shallower than the trenches; and

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a third region of the first conductivity type atop the first region, wherein a voltage on the conductive gate ~~control~~ controls a current flow from the third region through the first region to an underlying portion of the substrate.

10. (Currently Amended) The semiconductor device of claim [[1]] 2, wherein

the first region and the third region are in a first mesa between a first pair of the trenches; and

the second region is between a second pair of the trenches. [[;]]

11. (Original) The semiconductor device of claim 10, further comprising a fourth region of the second conductivity type, wherein the fourth region is at a surface of the substrate and extends across an entire separation between the second pair of trenches.

12. (Currently Amended) The semiconductor device of claim [[1]] 2, wherein a mesa between a first and a second of the trenches comprises:

the third region at a surface of the substrate and adjacent to the first trench;

a fourth region of the first conductivity type at the surface of the substrate and adjacent to the second trench;

a fifth region of the second conductivity type between the third and fourth regions at the surface of the substrate;

the first region underlying the third and fourth regions; and

the second region underlying the third region and separated from the first and second trenches.

13. (Original) The semiconductor device of claim 12, further comprising an electrical contact to the third, fourth, and fifth regions.

14. (Currently Amended) The semiconductor device of claim [[1]] 2, wherein the second region extends to a first plurality of adjacent mesas that are between pairs of the trenches and is absent from a second plurality of adjacent mesas that are between pairs of the trenches.

15. (Currently Amended) The semiconductor device of claim [[1]] 2, further

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comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the first region.

16. (Currently Amended) The semiconductor device of claim [[1]] 2, further comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the second region.

17. (Currently Amended) The semiconductor device of claim [[1]] 2, wherein the second region has a concentration of dopants of the second conductivity type that is higher than that of the first region.

Claims 18- 25 (Canceled)

26. (New) The semiconductor device of claim 2, wherein:

the first region forms a junction at the first depth; and

the second region forms a junction that is at the second depth and laterally separated from the trenches.

27. (New) The semiconductor device of claim 5, wherein the second junction is laterally separated from the trenches.

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